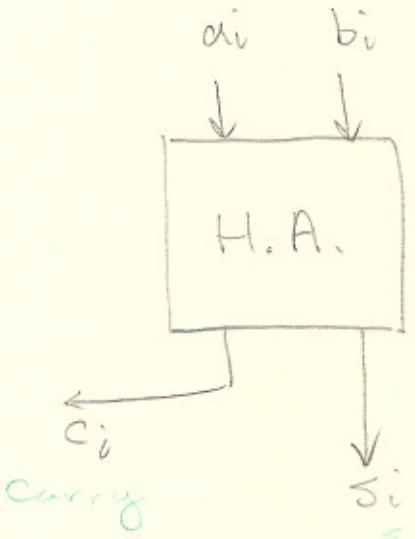
Half adder

A $a_{n-1} \ldots a_i \ldots a_1 a_0$

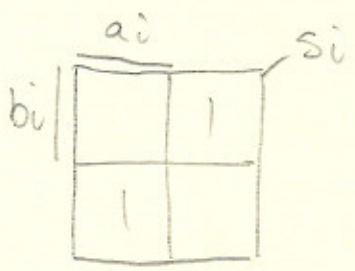
B $b_{n-1} \ldots b_i \ldots b_1 b_0$

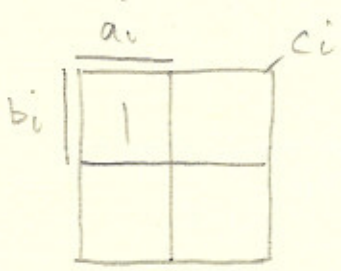
} registers



a_i	b_i	C_i	S_i
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

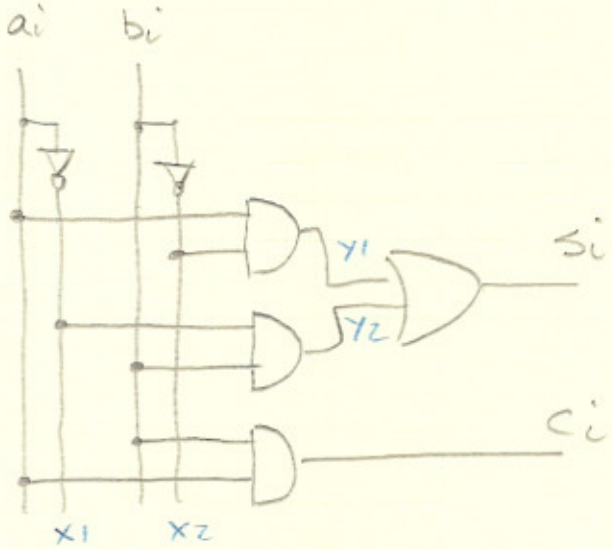
Step #1





Step # 2

$S_i = a_i \bar{b_i} + \bar{a_i} b_i$ $\quad C_i = a_i b_i$



Step # 3

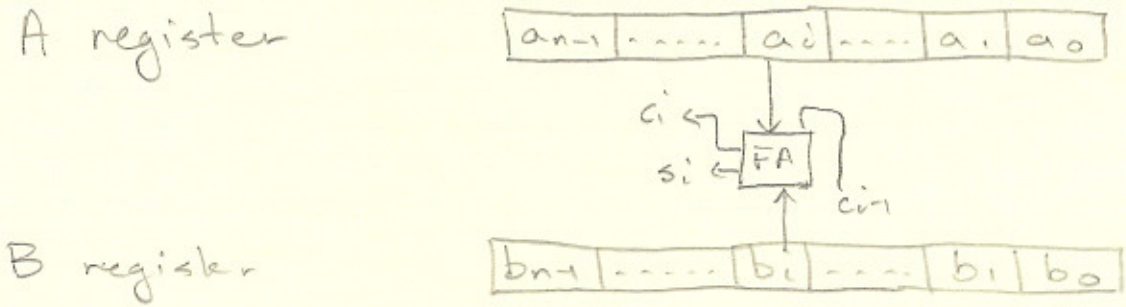
Design of C-mos circuit
(for homework)

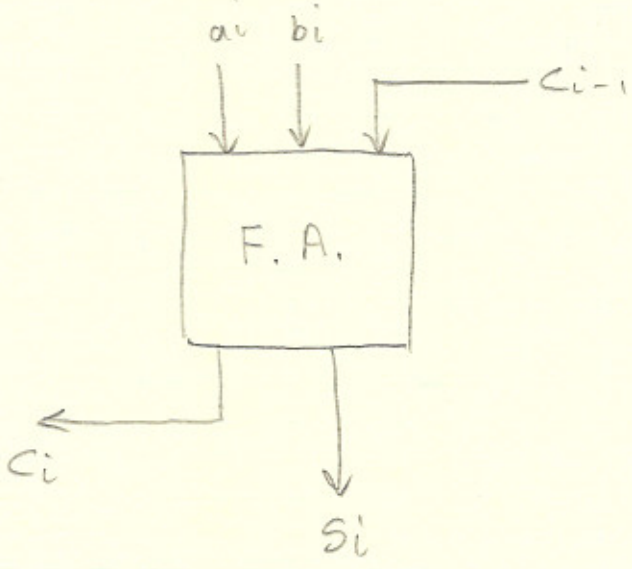
Step # 4

```
module half adder;
input AI, BI;
output SI, CI;
wire AI, BI, SI, CI, X1, X2, Y1, Y2;

begin

fork
X1 = !AI;
X2 = !BI;
join

#4;

fork
Y1 = AI && X2;
Y2 = BI && X1;
CI = AI && BI;
join

#4;

SI = Y1 || Y2;

#73
end
endmodule
```

Step # 5

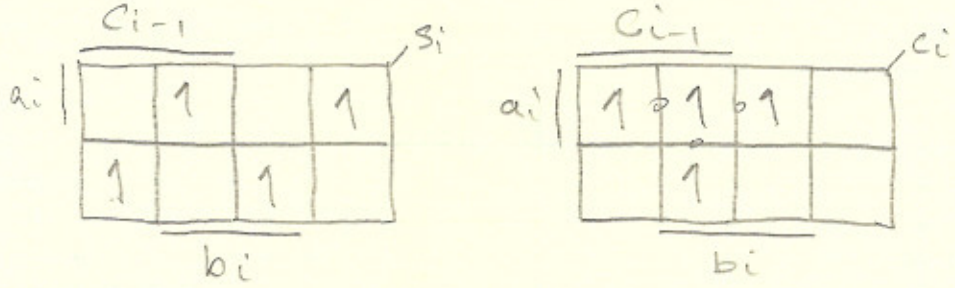
FULL ADDER





c_{i-1}	a_i	b_i	c_{i-1}	s_i
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

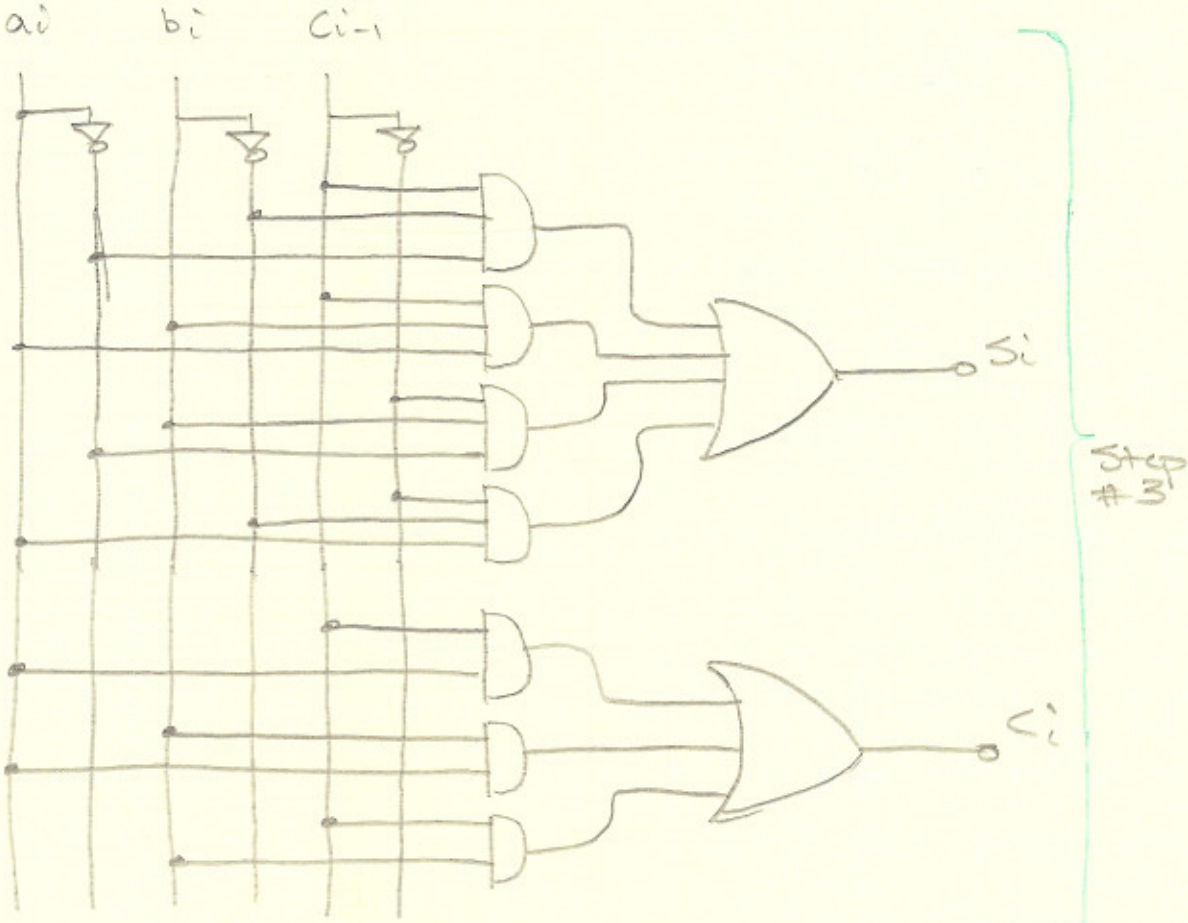
Step # 1



Step #2

$$S_i = C_{i-1}\,\bar{a}_i\,\bar{b}_i + C_{i-1}\,b_i\,a_i + \overline{C_{i-1}}\,\bar{a}_i\,b_i + \overline{C_{i-1}}\,a_i\,\bar{b}_i$$

$$C_i = C_{i-1}\,a_i + b_i\,a_i + C_{i-1}\,b_i$$



Step #3

Design C-MOS circuit (homework) } Step #4

```
module full adder;

inputs A1, B1, CI1;
outputs CI, SI;
wires A1, B1, CI1, CI, SI, X1, X2, X3, Y1, Y2, Y3
      Y4, Y5, Y6, Y7;

begin
fork
X1 = !A1;
X2 = !B2;
X3 = !CI1;
join
#4;

fork
Y1 = CI1 && X1 && X2;
Y2 = CI1 && A1 && B1;
Y3 = X3 && X1 && B1;
Y4 = X3 && A1 && X2;
Y5 = CI1 && A1;
Y6 = CI1 && B1;
Y7 = A1 && B1;
join
#4;
fork
SI = Y1 || Y2 || Y3 || Y4;
CI = Y5 || Y6 || Y7;
join
#4;

end
end module
```

Step #5